Figure 1

Flash Memory
Sensing
Block Diagram

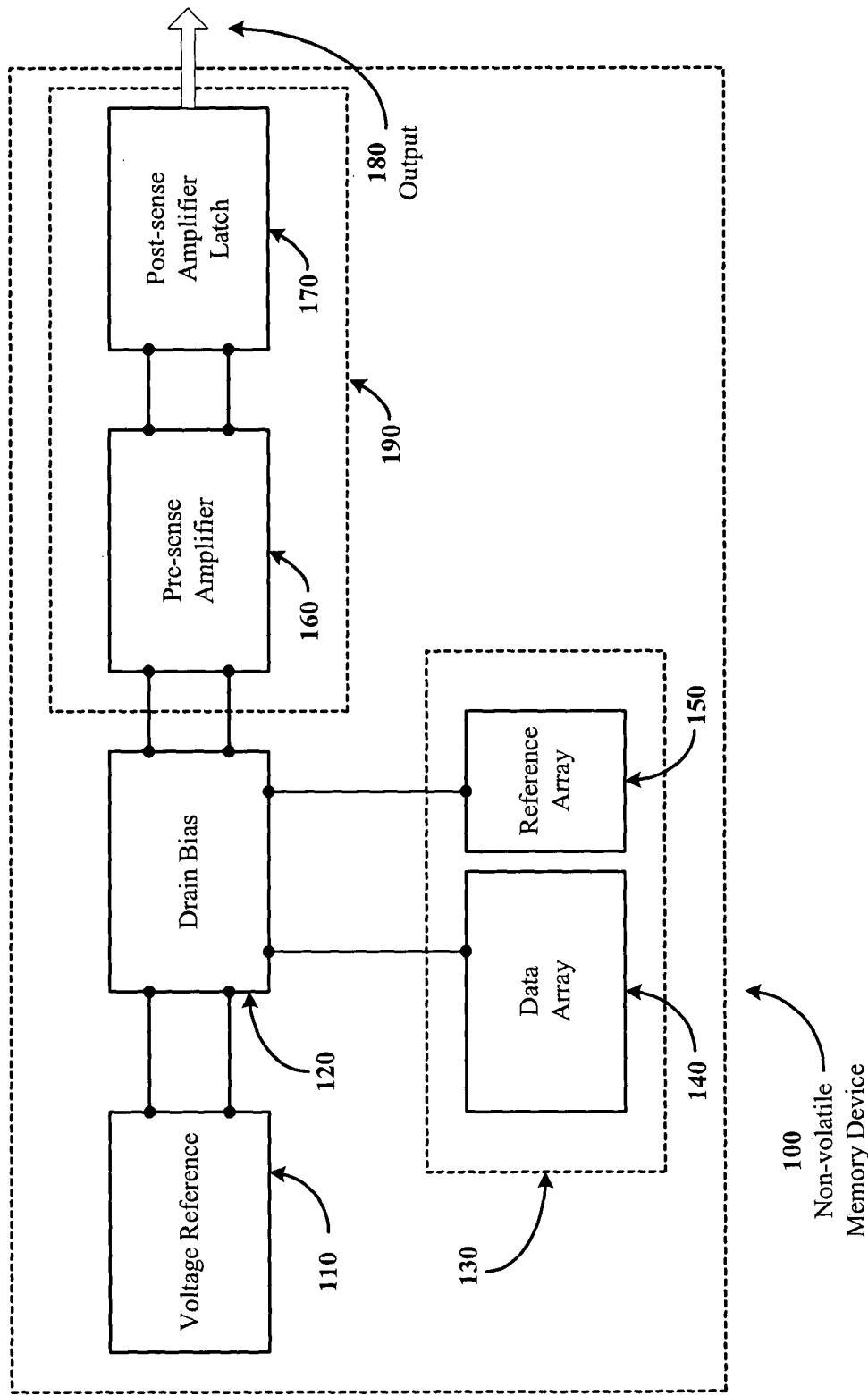
Voltage Reference
110

Drain Bias
120

Data Array
140

Reference Array
150

130

Pre-sense Amplifier
160

Post-sense Amplifier Latch
170

190

180 Output

100 Non-volatile Memory Device

Figure 2

Conventional
Feedback
Drain Bias Circuit

250
Voltage
Source

Vcc

210
Load

240
SIN/RIN Node --
Path to Sense Amplifier

200 s' Cascode Device

220
Biasing Feedback
Inverter

230
SEN/REN Node --
Path to Cell Drain

Figure 3

Static Reference
Drain
Bias Circuit

350
Voltage
Source

Vcc

310
Load

340
SIN/RIN Node --
Path to Sense Amplifier

320
·Drain Bias
Reference

300
n-Channel
Cascode Device

330
SEN/REN node --
Path to Cell Drain

440 Y Pump Voltage

460 Path to Referenced Circuit

455 Ground

450 Capacitor

445 Switching Device

430 p-Channel Device

435 Ground

465 Voltage Source

425 Cascode Device

470 N1 Node

420 Ground

V_cc

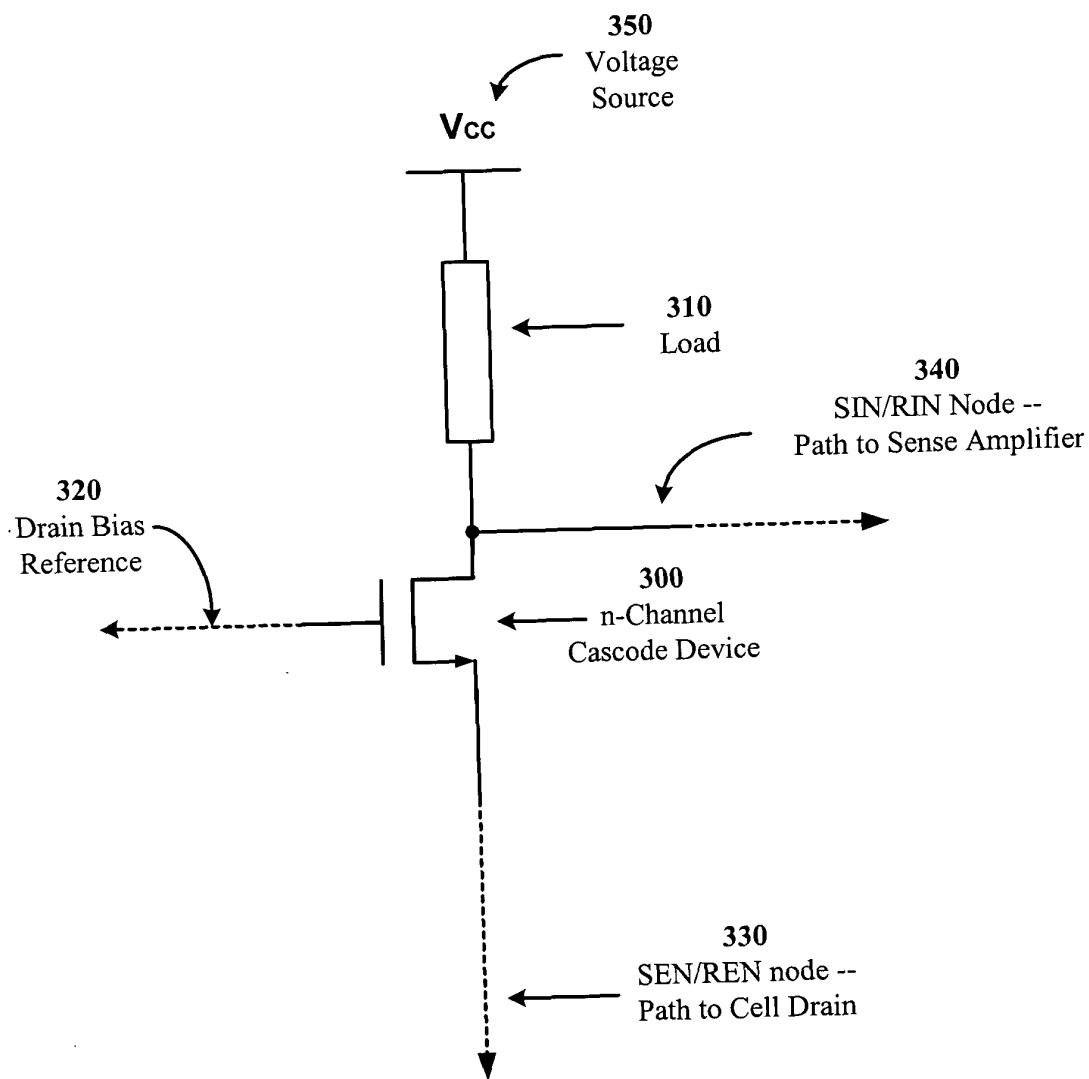**400** Differential Amplifier
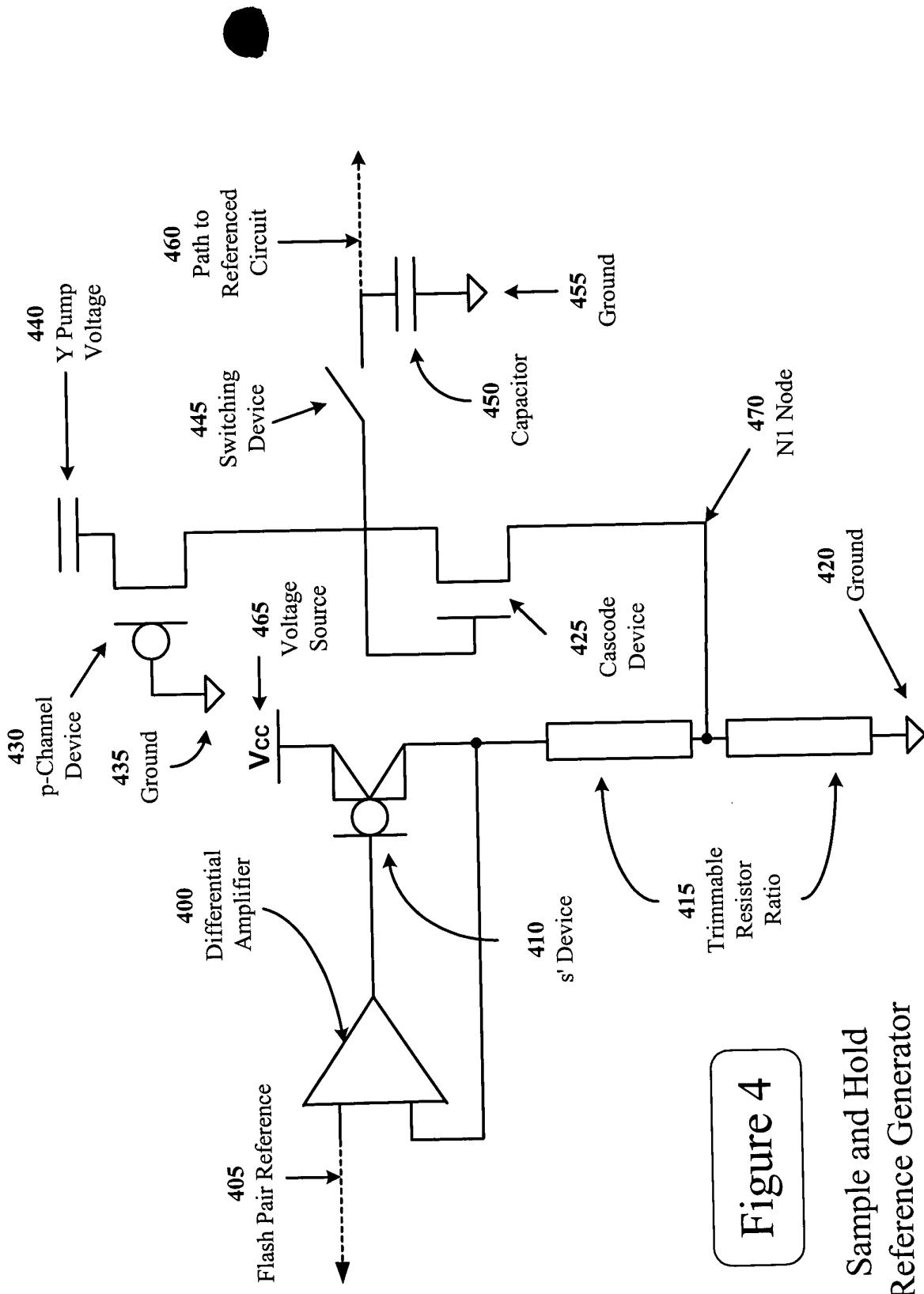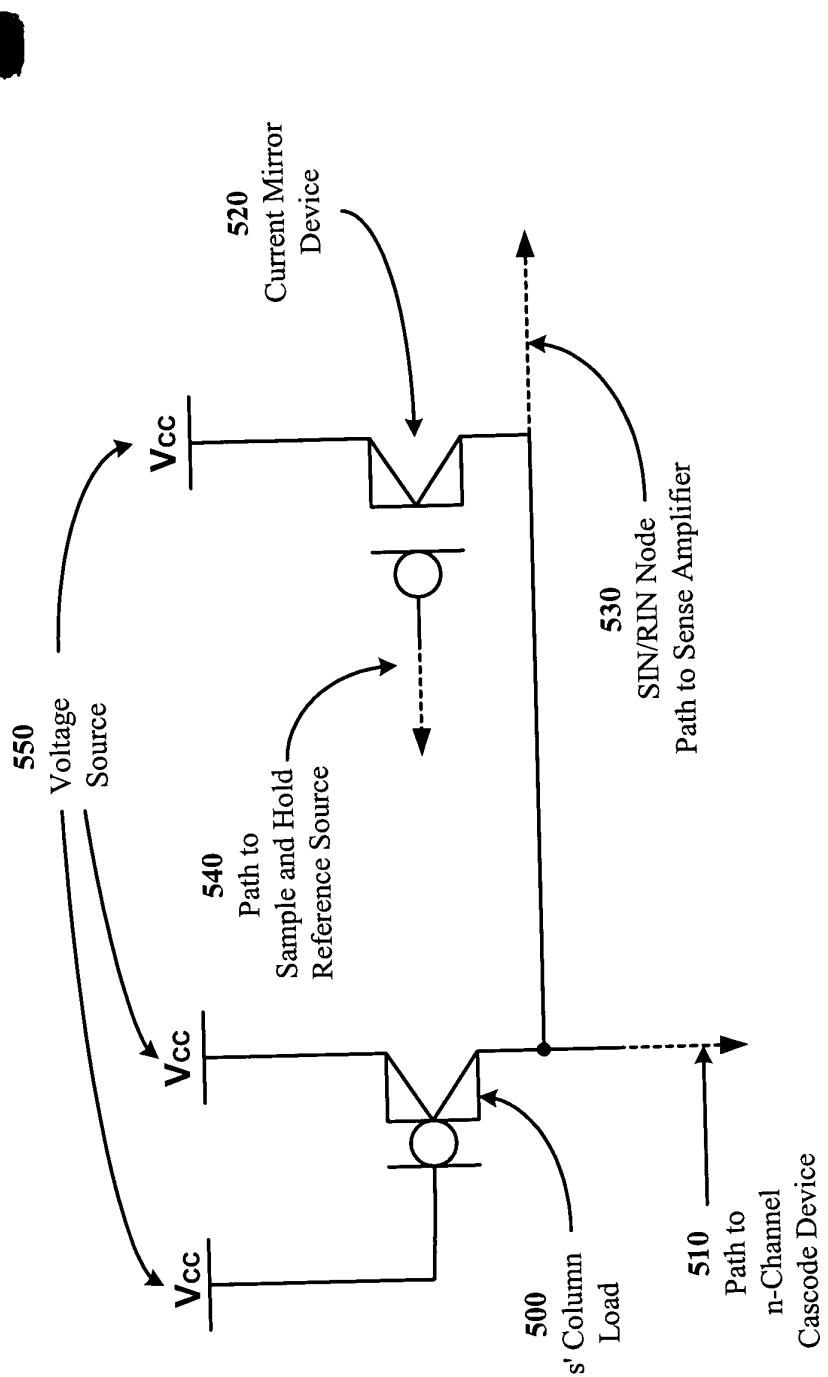
405 Flash Pair Reference

410 s' Device

415 Trimmable Resistor Ratio

Figure 4

Sample and Hold
Reference Generator

Drain Bias
Current Mirror and
Column Load with
Sample and Hold
Reference

520
Current Mirror
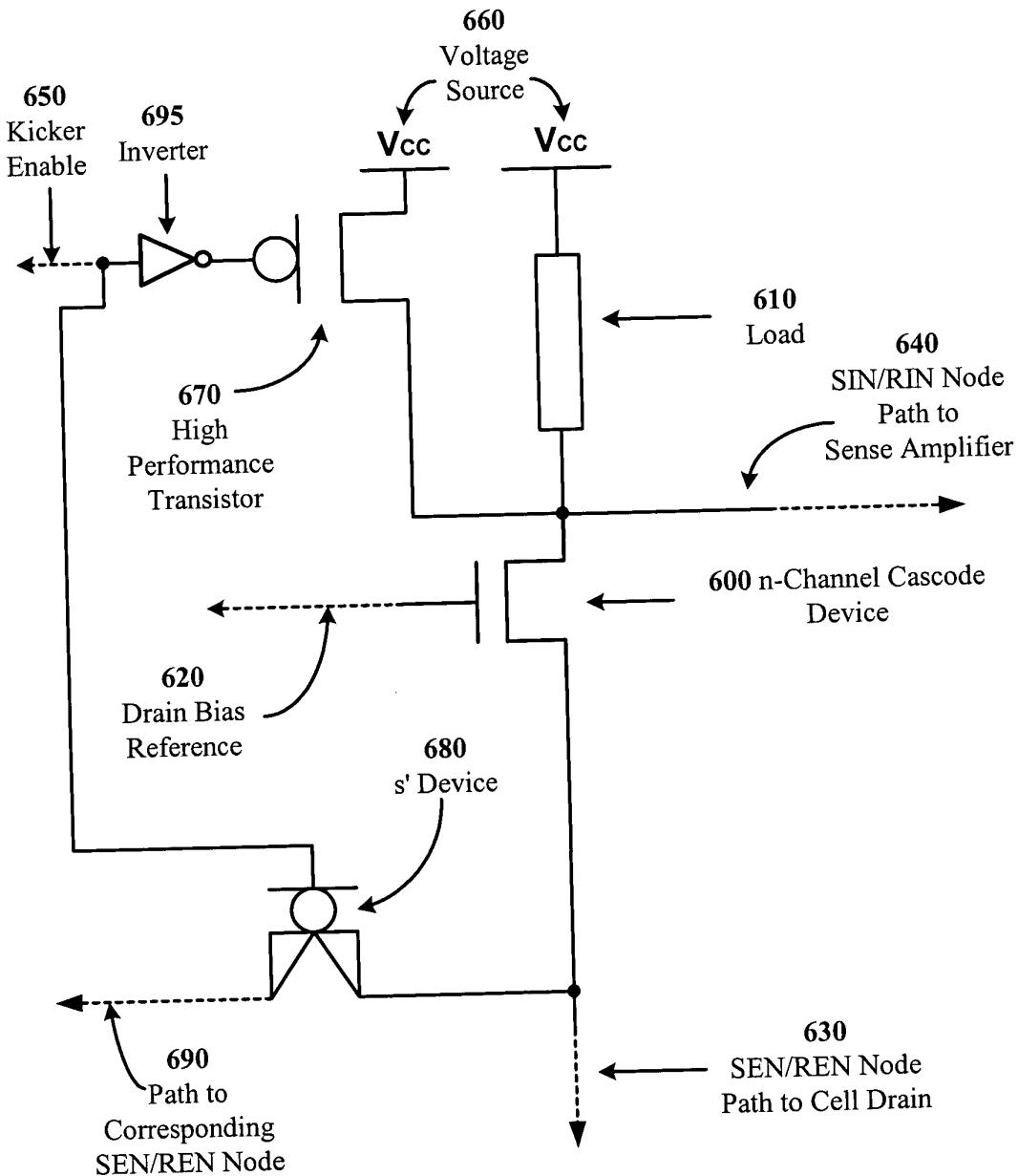Device

530
SIN/RIN Node
Path to Sense Amplifier

550
Voltage
Source

540
Path to
Sample and Hold
Reference Source

500
s' Column
Load

510
Path to
n-Channel
Cascode Device

V$_{CC}$

V$_{CC}$

V$_{CC}$

Figure 5

Figure 6

**Drain Bias
Kicker Circuit**

660
Voltage
Source

650
Kicker
Enable

695
Inverter

Vcc   Vcc

610
Load

640
SIN/RIN Node
Path to
Sense Amplifier

670
High
Performance
Transistor

600 n-Channel Cascode
Device

620
Drain Bias
Reference

680
s' Device

690
Path to
Corresponding
SEN/REN Node

630
SEN/REN Node
Path to Cell Drain

Figure 7

Drain Bias Pair
Circuit Diagram

710
Current Mirror
Sample and Hold
Reference

700

V_CC

705

V_CC

725 Filtered
VCC

715

V_CC

720

V_CC

735

V_CC

740

730

V_CC

780
SIN Node

745
Kicker
Enable

785
RIN Node

750

755

760
Cascode
Sample
and Hold
Reference

765

770 SEN Node

775 REN Node